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1 Simultaneous shield insertion and net ordering under explicit RLC noise constraint

Kevin M. Lepak, Irwan Luwandi, Lei He

June 2001 **Proceedings of the 38th conference on Design automation DAC '01**

Publisher: ACM Press

Full text available: pdf(152.11 KB) Additional Information: full citation, abstract, references, citings, index terms

For multiple coupled RLC nets, we formulate the min-area simultaneous shield insertion and net ordering SINO/NB-&ngr; problem to satisfy the given noise bound. We develop an efficient and conservative model to compute the peak noise, and apply the noise model to a simulated-annealing (SA) based algorithm for the SINO/NB-&ngr; problem. Extensive and accurate experiments show that the SA-based algorithm is efficient, and always achieves solutions satisfying the given noise bound. It uses up t ...

2 Efficient crosstalk noise modeling using aggressor and tree reductions

Li Ding, David Blaauw, Pinaki Mazumder

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design ICCAD '02**

Publisher: ACM Press

Full text available: pdf(139.91 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a fast method to estimate crosstalk noise in the presence of multiple aggressor nets for use in physical design automation tools. Since noise estimation is often part of the innerloop of optimization algorithms, very efficient closed-form solutions are needed. Previous approaches have typically used simple lumped 3--4 node circuit templates. One aggressor net is modeled at a time assuming that the coupling capacitances to all quiet aggressor nets are grounded. They also mode ...

3 Simultaneous shield insertion and net ordering for capacitive and inductive coupling minimization

Kevin M. Lepak, Min Xu, Jun Chen, Lei He

July 2004 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 9 Issue 3

Publisher: ACM Press

Full text available: pdf(308.22 KB) Additional Information: full citation, abstract, references, citings, index terms

In this article, we first show that existing net ordering formulations to minimize noise are no longer sufficient with the presence of inductive noise, and shield insertion is needed to minimize inductive noise. Using a K_{eff} model as the figure of merit for inductive coupling, we then formulate two simultaneous shield insertion and net ordering (SINO) problems: the optimal SINO/NF problem to find a minimal area SINO solution that is free of capacitive and inductive noise ...

Keywords: VLSI physical design automation, and on-chip inductance, net ordering, noise minimization, shielding, signal integrity

4 Signal and power delivery integrity: Top-k aggressors sets in delay noise analysis

Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester, Murat Becer
June 2007 **Proceedings of the 44th annual conference on Design automation DAC '07**
Publisher: ACM Press
Full text available: pdf(473.60 KB) Additional Information: full citation, abstract, references, index terms

We present, in this paper, novel algorithms to compute the set of "*top-k*" aggressors in a design. We show that the computation of the set of top-*k* aggressors is non-trivial, since we must consider all permutations of aggressors that are coupled to a critical path. Also, different sets of aggressors contribute different amounts of noise to each critical path and a brute-force enumeration to obtain the set of top-*k* aggressors has impractical runtime. Our proposed approach u ...

Keywords: crosstalk, delay noise, static timing analysis

5 Test generation for diagnosis, scan testing and advanced memory fault models: Interactive presentation: Automatic test pattern generation for maximal circuit noise in multiple aggressor crosstalk faults

Kunal P. Ganeshpure, Sandip Kundu
April 2007 **Proceedings of the conference on Design, automation and test in Europe DATE '07**
Publisher: EDA Consortium
Full text available: pdf(264.76 KB) Additional Information: full citation, abstract, references

Decreasing process geometries and increasing operating frequencies have made VLSI circuits more susceptible to signal integrity related failures. Capacitive crosstalk is one of the causes of such kind of failures. Crosstalk fault results from switching of neighboring lines that are capacitively coupled. Long nets are more susceptible to crosstalk faults because they tend to have a higher coupling capacitance to overall capacitance ratio. A typical long net has multiple aggressors. In generati ...

6 ClariNet: a noise analysis tool for deep submicron design

Rafi Levy, David Blaauw, Gabi Braca, Aurobindo Dasgupta, Amir Grinshpon, Chanlee Oh, Boaz Orshav, Supamas Sirichotiyakul, Vladimir Zolotov
June 2000 **Proceedings of the 37th conference on Design automation DAC '00**
Publisher: ACM Press
Full text available: pdf(101.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Coupled noise analysis has become a critical issue for deep-submicron, high performance design. In this paper, we present, ClariNet, an industrial noise analysis tool, which was developed to efficiently analyze large, high performance processor designs. We present the overall approach and tool flow of ClariNet and discuss three critical large-processor design issues which have received limited discussion in the past. First, we present how the

driver gates of a coupled interconnect network a ...

7 Efficient coupled noise estimation for on-chip interconnects

Anirudh Devgan

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design ICCAD '97**

Publisher: IEEE Computer Society

Full text available: pdf(46.07 KB) Publisher Site

Additional Information: full citation, abstract, references, citings, index terms

Noise analysis and avoidance is an increasingly critical step in deep submicron design. Ever increasing requirements on performance have led to widespread use of dynamic logic circuit families and its other derivatives. These aggressive circuit families trade off noise margin for timing performance making them more susceptible to noise failure and increasing the need for noise analysis. Currently, noise analysis is performed either through circuit or timing simulation or through model order redu ...

Keywords: Elmore delay, circuit simulation, coupled noise estimation, deep submicron design, dynamic logic circuit families, integrated circuit noise, noise analysis, noise criticality pruning, on-chip interconnects, physical design based noise avoidance, timing simulation

8 Pessimism reduction in crosstalk noise aware STA

M. Becer, V. Zolotov, R. Panda, A. Grinshpon, I. Algol, R. Levy, C. Oh

May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**

Publisher: IEEE Computer Society

Full text available: pdf(742.41 KB) Additional Information: full citation, abstract

High performance circuits are facing increasingly severe signal integrity problems due to crosstalk noise and crosstalk noise awareness has become an integral part of static timing analysis (STA). Existing crosstalk noise aware STA methods compute noise induced delay uncertainty on a net by net basis and in a pessimistic way, without considering the overlap bounds of the victim and aggressor timing windows and realistic delay impact on early and late signal arrival times. Since crosstalk induced ...

9 Using Prediction for Performance Optimization and Estimation: Early probabilistic noise estimation for capacitively coupled interconnects

Murat R Becer, David Blaauw, Ibrahim N. Hajj, Rajendran Panda

April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction SLIP '02**

Publisher: ACM Press

Full text available: pdf(306.85 KB) Additional Information: full citation, abstract, references, citings, index terms

One of the critical challenges in today's high performance IC design is to take noise into account as early as possible in the design cycle. Current noise analysis tools [1, 7} are effective at analyzing and identifying noise in the post-route design stage when detailed parasitic information is available. However, noise problems identified at this stage of design cycle are very difficult to fix due to the limited flexibility in the design and may cause additional iterations of routing and placem ...

Keywords: congestion, early noise analysis, global routing

10

False-noise analysis using logic implications

July 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 3

Publisher: ACM Press

Full text available: pdf(224.14 KB) Additional Information: full citation, abstract, references, index terms, review

Cross-coupled noise analysis has become a critical concern in today's VLSI designs. Typically, noise analysis makes the assumption that all aggressing nets can simultaneously switch in the same direction. This creates a worst- case noise pulse on the victim net that often leads to false noise violations. In this article we present a new approach that uses logic implications to identify the maximum set of aggressor nets that can inject noise simultaneously under the logic constraints of the circu ...

Keywords: VLSI (very large scale integration), circuit logic, noise analysis

11 Timing analysis and optimization: Crosstalk analysis using reconvergence correlation

Sachin Shrivastava, Rajendra Pratap, Harindranath Parameswaran, Manuj Verma

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press

Full text available: pdf(235.23 KB) Additional Information: full citation, abstract, references, index terms

In the UDSM era, crosstalk is an area of considerable concern for designers, as it can have a considerable impact on the yield, both in terms of functionality and operating frequency. Methods of crosstalk analysis are pessimistic in nature and the effort is ongoing to come up with techniques that make the analysis as realistic as possible. Using information from timing analysis is one such technique where we use data about overlap in switching among nets to identify those that can potentially sw ...

12 Session 8D: Timing and noise analysis: False-noise analysis using logic implications

Alexey Glebov, Sergey Gavrilov, David Blaauw, Supamas Sirichotiyakul, Chanhee Oh, Vladimir Zolotov

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design ICCAD '01**

Publisher: IEEE Press

Full text available: pdf(133.42 KB) Additional Information: full citation, abstract, references, citings, index terms

Cross-coupled noise analysis has become a critical concern in today's VLSI designs. Typically, noise analysis makes an assumption that all aggressing nets can simultaneously switch in the same direction. This creates a worst-case noise pulse on the victim net that often leads to false noise violations. In this paper, we present a new approach that uses logic implications to identify the maximum set of aggressor nets that can inject noise simultaneously under the logic constraints of the circuit. ...

13 Issues in crosstalk: Efficient switching window computation for cross-talk noise

Bhavana Thudi, David Blaauw

December 2002 **Proceedings of the 8th ACM/IEEE international workshop on Timing issues in the specification and synthesis of digital systems TAU '02**

Publisher: ACM Press

Full text available: pdf(182.45 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we present an efficient method for computing switching windows in the presence of delay noise. In static timing analysis, delay noise has traditionally been modeled using a simple switch-factor based noise model and the computation of switching

windows is performed using an iterative algorithm where timing window propagation and switch factor updates are computed repeatedly until convergence. It was shown that the worst-case number of iterations required for convergence is O(n< ...

14 Novel design methodologies and signal integrity: Static noise analysis with noise windows

Ken Tseng, Vinod Kariat

June 2003 **Proceedings of the 40th conference on Design automation DAC '03**

Publisher: ACM Press

Full text available: pdf(122.54 KB) Additional Information: full citation, abstract, references, citings, index terms

As processing technology scales down to the nanometer regime, capacitive crosstalk is having an increasingly adverse effect on circuit functionality, leading to increasing number of chip failures. In this paper, we propose mapping the static crosstalk functional noise problem into the well understood static timing problem. The key differences between static noise and static timing analyses, namely the injection of noise, accurate noise window propagation and register sensitive window computation ...

Keywords: crosstalk, noise, signal integrity

15 Poster Paper Introductions: Crosstalk noise optimization by post-layout transistor sizing

Masanori Hashimoto, Masao Takahashi, Hidetoshi Onodera

April 2002 **Proceedings of the 2002 international symposium on Physical design ISPD '02**

Publisher: ACM Press

Full text available: pdf(157.68 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper proposes a post-layout transistor sizing method for crosstalk noise reduction. The proposed method downsizes the drivers of the aggressor wires for noise reduction, utilizing the precise interconnect information extracted from the detail-routed layouts. We develop a transistor sizing algorithm for crosstalk noise reduction under delay constraints, and construct a crosstalk noise optimization method utilizing a crosstalk noise estimation method and a transistor sizing framework which a ...

Keywords: capacitive coupling noise, crosstalk noise, gate sizing, post-layout optimization, transistor sizing

16 Dynamic Noise Analysis with Capacitive and Inductive Coupling

Seung Hoon Choi, Bipul C. Paul, Kaushik Roy

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design ASP-DAC '02**

Publisher: IEEE Computer Society

Full text available: pdf(334.88 KB) Publisher Site Additional Information: full citation, abstract

In this paper we propose a dynamic noise model to verify functional failures due to crosstalk in high-speed circuits. Conventional DC noise analysis produces pessimistic results because it ignores the fact that a gate acts as a low-pass filter. In contrast, the dynamic noise model considers the temporal property of a noise waveform and analyzes its effect on functionality. In this model, both capacitive and inductive coupling are considered as the dominant source of noise in high-speed deep-subm ...

Keywords: crosstalk, noise analysis, capacitiance, inductance, noise model, dynamic noise margin, deep submicron

17 An efficient sequential quadratic programming formulation of optimal wire spacing for cross-talk noise avoidance routing

Paul B. Morton, Wayne Dai

April 1999 **Proceedings of the 1999 international symposium on Physical design ISPD '99**

Publisher: ACM Press

Full text available: pdf(857.65 KB) Additional Information: full citation, references, citings, index terms

18 Cross-talk noise analysis and management: Crosstalk noise estimation for noise management

Paul B. Morton, Wayne Dai

June 2002 **Proceedings of the 39th conference on Design automation DAC '02**

Publisher: ACM Press

Full text available: pdf(288.08 KB) Additional Information: full citation, abstract, references, index terms

One of the main challenges in developing an effective crosstalk noise management strategy is to develop a crosstalk noise estimate which is both accurate and leads to a tractable optimization problem that can be used to optimally redistribute uncommitted routing resources to resolve crosstalk noise violations. Devgan's [4] estimate comes very close to meeting these objectives, however, it is extremely pessimistic for nets with long couplings or aggressor nets with short rise times. The increased ...

Keywords: crosstalk, estimation, local approximation, noise, noise management, optimal spacing

19 Routing techniques: Routing of analog busses with parasitic symmetry

Lars Schreiner, Markus Olbrich, Erich Barke, Volker Meyer zu Bexten

April 2005 **Proceedings of the 2005 international symposium on Physical design ISPD '05**

Publisher: ACM Press

Full text available: pdf(591.16 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a new methodology for routing net bundles like busses and paired nets maintaining parasitic symmetry. It is mainly devoted to analog signal interconnect and can also be used for critical digital busses or clock signals. The PARasitic SYmmetric router (PARSY) is the first router that limits differential capacitances to a user defined value. Wirelength differences inside a net bundle are also equalized automatically. This routing methodology uses a novel module generator approa ...

Keywords: EDA, IC-layout, RF, analog routing, bus routing, net bundles, paired nets, routing, virtual terminals

20 Cross-talk noise analysis and management: Variable frequency crosstalk noise analysis: a methodology to guarantee functionality from dc to f_{max}

Byron Krauter, David Widiger

June 2002 **Proceedings of the 39th conference on Design automation DAC '02**

Publisher: ACM Press

One means of reducing pessimism in crosstalk analysis is to consider timing orthogonality. While earlier works have addressed the temporal alignment of timing windows [1, 2, 3, 4], these treatments have overlooked one key point. Crosstalk noise failures are frequency dependent. A chip that functions at one frequency can fail due to crosstalk noise at faster and slower frequencies. Moreover, because system developers and manufacturers need chips that operate over a wide range of frequencies, nois ...

Keywords: GCD frequency, LCM window, crosstalk, frequency-dependent noise, noise analysis, timing orthogonality, timing windows

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